

REMARKS

Examiner J. Maldonado is thanked for the thorough examination and search of the subject Patent Application. Claims 1, 2, 7, 8, 9, 15, and 18 have been amended. Claims 4, 13, 14, 16, and 22 have been canceled.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 1-3 and 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Liu (U.S. 5,693,568) is requested based on Amended Claims 1 and 2, and on the following remarks.

Applicant has amended Claim 1 to include the limitations of a using a first metal layer, an etch stop layer, and a second metal layer where the etch stop layer comprises a tungsten containing film. Amended Claim 1 is shown below as:

1. (Currently Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

5 depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a tungsten containing film;

10 depositing a second metal layer overlying said etch stop layer;

 etching through said second metal layer, said etch stop layer, and said first metal layer to form connective lines;

15 thereafter etching partially through said second metal layer to form vias;

 thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

20 polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device.

Applicant notes that the use of a tungsten containing film is described in the original Specification on page 8 in the paragraph shown below:

"An etch stop layer 62 is deposited overlying the first

metal layer 58. The purpose of the etch stop layer 62 is to allow complete etching through of the second metal layer 66 without damaging the underlying first metal layer 58. The etch stop layer 62 preferably comprises one of the group of: titanium nitride (TiN), titanium (T), **tungsten (W)**, **tungsten nitride (WN)**, **tantalum (Ta)**, and **tantalum nitride (TaN)**. The etch stop layer 62 is optional to the present invention. In the case where the etch stop layer 62 is not used, a timed etch must be used to allow independent etching of the first and second metal layers."

Further, Applicant has reviewed the cited art and has found the following regarding the use of an etch stop layer:

- (1) Rhodes et al teaches an etch barrier layer 6 (Fig. 1) comprising chromium (Col. 2, lines 45-47).
- (2) Liu et al teaches an etch stop layer 8 (Fig. 1) comprising titanium nitride (Col. 6, lines 57-62).
- (3) Wang et al (US Patent 6,080,660) teaches an etch stop layer 24 comprising a composite titanium/titanium nitride layer (Col. 3, line 65 through Col. 4, line 2).

Based on this analysis, Applicant finds that the cited

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prior art does not teach nor suggest, individually or in combination, the use of a tungsten containing film as the etch stop layer as found in Applicant's claimed invention recited as Amended Claim 1. It would not have been obvious to one skilled in the art at the time of the invention to have practiced the invention as recited by Applicant's Amended Claim 1. Therefore, Applicant respectfully requests that the rejection of Claim 1 under 35 USC 103(a) be removed. Claim 2 has been amended to correspond to the new language of Amended Claim 1. Claims 2-3, and 6 contain patentably distinct, further limitations on base Claim 1 and should be in condition for allowance if the rejection of Amended Claim 1 is removed.

Reconsideration of Claims 1-3 and 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Liu (U.S. 5,693,568) is requested based on Amended Claims 1 and 2, and on the above remarks.

Reconsideration of Claims 5, 7, and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Liu (U.S. 5,693,568) and further in view of Wang et al (U.S. 6,080,660) is requested based on Amended Claims 1, 7, and 8, and on the following remarks.

Based on this analysis above, Applicant finds that the cited prior art does not teach nor suggest, individually or in combination, the use of a tungsten containing film as the etch stop layer as found in Applicant's claimed invention recited as Amended Claim 1. It would not have been obvious to one skilled in the art at the time of the invention to have practiced the invention as recited by Applicant's Amended Claim 1. Therefore, Applicant respectfully requests that the rejection of Claim 1 under 35 USC 103(a) be removed. Claims 7 and 8 have been amended to correspond to the new language of Amended Claim 1. Claims 5, 7, and 8 contain patentably distinct, further limitations on base Claim 1 and should be in condition for allowance if the rejection of Amended Claim 1 is removed.

Reconsideration of Claims 5, 7, and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Liu (U.S. 5,693,568) and further in view of Wang et al (U.S. 6,080,660) is requested based on Amended Claims 1, 7, and 8, and on the above remarks.

Reconsideration of Claims 9-12 and 14-23 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Liu (U.S. 5,693,568) and in view of Wang et al (U.S. 6,080,660) is requested based on Amended Claims 9,

15, and 18, Canceled Claims 14, 16, and 22, and on the following remarks.

Independent Claims 9 and 18 have been amended to include the limitations of a using a first metal layer, an etch stop layer, and a second metal layer where the etch stop layer comprises a tantalum containing film. Amended Claim 9 is shown below as:

9. (Currently Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

5 depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a tantalum containing film;

10 depositing a second metal layer overlying said ~~first metal layer etch stop layer~~;

~~depositing an anti-reflective coating layer comprising titanium nitride (TiN) overlying said second metal layer;~~
~~etching through said anti-reflective coating layer,~~

15 said second metal layer, said etch stop layer, and said
 first metal layer to form connective lines;
 thereafter etching through ~~said anti-reflective~~
 ~~coating layer~~ and said second metal layer to form vias;
 thereafter depositing a dielectric layer overlying
20 said vias, said connective lines and said semiconductor
 substrate; and
 polishing down said dielectric layer to complete said
 self-aligned, anti-via interconnects in the manufacture of
 the integrated circuit device wherein said anti-reflective
25 coating layer is a polishing stop.

Amended Claim 18 is shown below as:

18. (Currently Amended) A method of forming self-aligned,
 anti-via interconnects in an integrated circuit device
 comprising:

 providing a semiconductor substrate;
5 depositing a first metal layer overlying said
 semiconductor substrate;
 depositing an etch stop layer overlying said first
 metal layer wherein said etch stop layer comprises a
 tantalum containing film;

10 depositing a second metal layer overlying said first
metal layer;

 depositing an anti-reflective coating layer comprising
titanium nitride (TiN) overlying said second metal layer;

15 etching through said anti-reflective coating layer,
 said second metal layer, said etch stop layer, and said
second metal layer to form connective lines;

 thereafter etching through said anti-reflective
coating layer and said second metal layer to form vias
wherein said etch stop layer acts as an etch stop;

20 thereafter depositing a dielectric layer overlying
said vias, said connective lines and said semiconductor
substrate; and

 polishing down said dielectric layer to complete said
self-aligned, anti-via interconnects in the manufacture of
25 the integrated circuit device wherein said anti-reflective
coating layer is a polishing stop.

Based on this analysis above, Applicant finds that the cited prior art does not teach nor suggest, individually or in combination, the use of a tantalum containing film as the etch stop layer as found in Applicant's claimed invention recited as Amended Claims 9 and 18. It would not have been obvious to one skilled in the art at the time of the invention to have

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practiced the invention as recited by Applicant's Amended Claims 9 and 18. Therefore, Applicant respectfully requests that the rejection of Claims 9 and 18 under 35 USC 103(a) be removed. Claim 15 has been amended to correspond to the new language of Amended Claim 9. Claims 14, 16, and 22 have been canceled. Claims 10-12, 15 and 16 contain patentably distinct, further limitations on base Claim 9 and should be in condition for allowance if the rejection of Amended Claim 9 is removed. Claims 19-21 and 23 contain patentably distinct, further limitations on base Claim 18 and should be in condition for allowance if the rejection of Amended Claim 18 is removed.

Reconsideration of Claims 9-12 and 14-23 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Liu (U.S. 5,693,568) and in view of Wang et al (U.S. 6,080,660) is requested based on Amended Claims 9, 15, and 18, Canceled Claims 14, 16, and 22, and on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and have discussed their impact on the present invention above.

Allowance of all Claims is requested.

It is requested that should Examiner V. Yevsikov not find that the Claims are now Allowable that the Examiner call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,



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